

07/31/98

JCS531 U.S. PTO

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PTO/SB/05 (12/97)
Approved for use through 09/30/00. OMB 0651-0032
Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCEUTILITY
PATENT APPLICATION
TRANSMITTAL

Attorney Docket No. 02282.P055

Total Pages 1

First Named Inventor or Application Identifier

Alain Raynaud

Express Mail Label No.

EM542801726US

(Only for new nonprovisional applications under 37 CFR 1.53(b))

APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents.

ADDRESS TO:

Assistant Commissioner for Patents
Box Patent Application
Washington, DC 20231

1. ☒ Fee Transmittal Form
(Submit an original, and a duplicate for fee processing)
2. ☒ Specification [Total Pages 44]
(preferred arrangement set forth below)
 - Descriptive title of the invention
 - Cross References to Related Applications
 - Statement Regarding Fed sponsored R & D
 - Reference to Microfiche Appendix
 - Background of the invention
 - Brief Summary of the invention
 - Brief Description of the Drawings (if filed)
 - Detailed Description
 - Claim(s)
 - Abstract of the Disclosure
3. ☒ Drawing(s) (35 USC 113) [Total Sheets 20]
4. Oath or Declaration (unsigned) [Total Pages 4]
 - a. ☒ Newly executed (original or copy)
 - b. ☐ Copy from a prior application (37 CFR 1.63(d))
(for continuation/divisional with Box 17 completed)
(Note Box 5 below)
 - i. ☐ DELETION OF INVENTOR(S)
Signed statement attached deleting inventor(s) named in the prior application, see 37 CFR 1.63(d)(2) and 1.33(b).
5. ☐ Incorporation By Reference (useable if Box 4b is checked)
The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4b, is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein.

6. ☐ Microfiche Computer Program (Appendix)
7. Nucleotide and/or Amino Acid Sequence Submission (if applicable, all necessary)
 - a. ☐ Computer Readable Copy
 - b. ☐ Paper Copy (identical to computer copy)
 - c. ☐ Statement verifying identity of above copies

ACCOMPANYING APPLICATION PARTS

8. ☐ Assignment Papers (cover sheet & document(s))
9. ☐ 37 CFR 3.73(b) Statement ☐ Power of Attorney
(when there is an assignee)
10. ☐ English Translation Document (if applicable)
11. ☐ Information Disclosure Statement (IDS)/PTO-1449 ☐ Copies of IDS Citations
12. ☐ Preliminary Amendment
13. ☒ Return Receipt Postcard (MPEP 503)
(Should be specifically itemized)
14. ☐ Small Entity ☐ Statement filed in prior application, Status still proper and desired
15. ☐ Certified Copy of Priority Document(s)
(if foreign priority is claimed)
16. ☒ Other: Certificate of Mailing

17. If a CONTINUING APPLICATION, check appropriate box and supply the requisite information:

☐ Continuation ☐ Divisional ☐ Continuation-in-part (CIP) of prior application No: _____/_____

18. CORRESPONDENCE ADDRESS

☐ Customer Number or Bar Code Labelor ☒ Correspondence address below

(Insert Customer No. or Attach bar code label here):

NAME	William D. Davis				
	Blakely Sokoloff Taylor & Zafman, LLP				
ADDRESS	12400 Wilshire Blvd.				
	Seventh Floor				
CITY	Los Angeles	STATE	California	ZIP CODE	90025
COUNTRY	United States	TELEPHONE	503-684-6200	FAX	503-684-3245

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PTO/SB/17 (12-97)

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Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE

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FEE TRANSMITTALNote: Effective October 1, 1997.
Patent fees are subject to annual revision.TOTAL AMOUNT OF PAYMENT (\$)**1,568.00****Complete if Known**

Application Number	
Filing Date	July 31, 1998
First Named Inventor	Alain Raynaud
Group Art Unit	
Examiner Name	
Attorney Docket Number	02282.P055

METHOD OF PAYMENT (check one)

- 1.
- ☒
- The Commissioner is hereby authorized to charge indicated fees and credit any over payments to:

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Number
Deposit
Account
Name**02-2666**

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- Charge Any Additional Fee Required Under 37 CFR 1.16 and 1.17
- ☐
- Charge the Issue Fee Set in 37 CFR 1.18 at the Mailing of the Notice of Allowance

- 2.
- ☒
- Payment Enclosed:

☒ Check
 ☐ Money Order
 ☐ Other
FEE CALCULATION**1. FILING FEE**

Large Entity Fee Code (\$)	Small Entity Fee Code (\$)	Fee Description	Fee Paid
101 790	201 395	Utility filing fee	790.00
106 330	206 165	Design filing fee	
107 540	207 270	Plant filing fee	
108 790	208 395	Reissue filing fee	
114 150	214 75	Provisional filing fee	

SUBTOTAL (1) (\$)**790.00****2. CLAIMS**

Total Claims	Extra	Fee from below	Fee Paid
33	-20 =	13 X 22 =	286.00
9	-3 =	6 X 82 =	492.00
Multiple Dependent Claims			

Large Entity Fee Code (\$)	Small Entity Fee Code (\$)	Fee Description
103 22	203 11	Claims in excess of 20
102 82	202 41	Independent claims in excess of 3
104 270	204 135	Multiple dependent claim
109 82	209 41	Reissue independent claims over original patent
110 22	210 11	Reissue claims in excess of 20 and over original patent

SUBTOTAL (2) (\$)**778.00****FEE CALCULATION (continued)****3. ADDITIONAL FEES**

Large Entity Fee Code (\$)	Small Entity Fee Code (\$)	Fee Description	Fee Paid
105 130	205 65	Surcharge - late filing fee or oath	
127 50	227 25	Surcharge - late provisional filing fee or cover sheet	
139 130	139 130	Non-English specification	
147 2,520	147 2,520	For filing a request for reexamination	
112 920*	112 920*	Requesting publication of SIR prior to Examiner action	
113 1,940*	113 1,940*	Requesting publication of SIR after Examiner action	
115 110	215 55	Extension for reply within first month	
116 400	216 200	Extension for reply within second month	
117 950	217 475	Extension for reply within third month	
118 1,510	218 755	Extension for reply within fourth month	
128 2,060	228 1,030	Extension for reply within fifth month	
119 310	219 155	Notice of Appeal	
120 310	220 155	Filing a brief in support of an appeal	
121 270	221 135	Request for oral hearing	
138 1,510	138 1,510	Petition to institute a public use proceeding	
140 110	240 55	Petition to revive - unavoidable	
141 1,320	241 660	Petition to revive - unintentional	
142 1,320	242 660	Utility issue fee (or reissue)	
143 450	243 225	Design issue fee	
144 670	244 335	Plant issue fee	
122 130	122 130	Petitions to the Commissioner	
123 50	123 50	Petitions related to provisional applications	
126 240	126 240	Submission of Information Disclosure Stmt	
581 40	581 40	Recording each patent assignment per property (times number of properties)	
146 790	246 395	Filing a submission after final rejection (37 CFR 1.129(a))	
149 790	249 395	For each additional invention to be examined (37 CFR 1.129(b))	
Other fee (specify) _____			
Other fee (specify) _____			

* Reduced by Basic Filing Fee Paid

SUBTOTAL (3) (\$)**0.00****SUBMITTED BY**Typed or Printed Name **William D. Davis**Signature **William D. Davis**Date **7/31/98****Complete (if applicable)**Reg. Number **38,428**

Deposit Account User ID

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09154-07160

Our Reference: 02282.P055

Patent

METHOD AND APPARATUS FOR GATE-LEVEL SIMULATION OF SYNTHESIZED REGISTER TRANSFER LEVEL DESIGNS WITH SOURCE-LEVEL DEBUGGING

Inventors: Alain Raynaud and Luc M. Burgun

Respectfully submitted,

BLAKELY SOKOLOFF TAYLOR & ZAFMAN LLP

William D. Davis

William D. Davis

Reg. No. 38,428

"Express Mail" mailing label number: EM542801726US

Date of Deposit: July 31, 1998

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Michelle J. Turner

(Typed or printed name of person mailing paper or fee)

(Signature of person mailing paper or fee)

(Date signed)

Serial/Patent No.: <u>****</u>	Filing/Issue Date: <u>July 31, 1998</u>
Client: <u>Mentor Graphics (Raynaud, et al.)</u>	
Title: <u>Method and Apparatus for Gate-Level Simulation of Synthesized Register Transfer Level Designs with Source-Level Debugging</u>	
BSTZ File No.: <u>02282.P055</u>	Atty/Secty Initials: <u>WDD/mit</u>
Date Mailed: <u>July 31, 1998</u>	Docket Due Date: <u>*****</u>
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<input type="checkbox"/> Amendment/Response (____ pgs.)	<input checked="" type="checkbox"/> Express Mail No.: <u>EM542801726US</u> <input checked="" type="checkbox"/> Check No. <u>5472</u>
<input checked="" type="checkbox"/> Appeal Brief (____ pgs.) (in triplicate)	<input type="checkbox"/> _____ Month(s) Extension of Time Amt: <u>\$1568.00</u>
<input checked="" type="checkbox"/> Application - Utility (<u>44</u> pgs., with cover and abstract)	<input type="checkbox"/> Information Disclosure Statement & PTO-1449 (____ pgs.) <input type="checkbox"/> Check No. _____
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<input type="checkbox"/> Application - Rule 1.60 CIP (____ pgs.)	<input type="checkbox"/> Petition for Extension of Time
<input type="checkbox"/> Application - Rule 1.62 Transmittal (____ pgs.)	<input checked="" type="checkbox"/> Petition for _____
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<input type="checkbox"/> Application - PCT (____ pgs.)	<input type="checkbox"/> Power of Attorney (____ pgs.)
<input type="checkbox"/> Application - Provisional (____ pgs.)	<input type="checkbox"/> Preliminary Amendment (____ pgs.)
<input type="checkbox"/> Assignment and Cover Sheet	<input type="checkbox"/> Reply Brief (____ pgs.)
<input checked="" type="checkbox"/> Certificate of Mailing	<input type="checkbox"/> Response to Notice of Missing Parts
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<input type="checkbox"/> Disclosure Docs & Orig & Copy of Inventor's Signed Letter (____ pgs.)	<input type="checkbox"/> Small Entity Declaration for Indep. Inventor/Small Business
<input checked="" type="checkbox"/> Drawings: <u>20</u> # of sheets includes <u>22</u> figures	<input checked="" type="checkbox"/> Transmittal Letter (original & copy) x 1 page each
<input checked="" type="checkbox"/> Other: Fee transmittal (original & copy) x 1 page each	

Update

Search for Application Number 09/127,584

First Search:

Update Search: X

Date: 8/8/00

Background Info

Effective Filing Date

Inventor

Assignee

Raynaud et al.

Title

Search

Classes/Subclasses

See File Wrapper

East Search

1	((RTL SAME DEBUG\$4) AND BREAKPOINT)	USPAT 2000/08/08 12:53
29	(RTL AND ((SIMULAT\$3 NEAR CIRCUIT)) AND DEBUG\$4)	USPAT 2000/08/08 12:53
1	((RTL SAME DEBUG\$4) AND BREAKPOINT)	USPAT 2000/08/08 12:53
34	((RTL AND DEBUG\$4) AND (SIMULAT\$3 NEAR CIRCUIT))	USPAT 2000/08/08 12:53
22	((((RTL AND ((SIMULAT\$3 NEAR CIRCUIT)) AND DEBUG\$4)) AND BREAK)	USPAT 2000/08/08 13:07
23	((RTL AND DEBUG\$4) AND (SIMULAT\$3 NEAR CIRCUIT) AND BREAK\$)	USPAT 2000/08/08 13:08
6	((VHDL OR RTL OR HDL) AND (SOURCE ADJ LEVEL ADJ DEBUG\$4))	USPAT 2000/08/08 13:11
15	(DESIGN ADJ ANNOTAT\$3)	USPAT 2000/08/08 13:12
5	((((SOURCE ADJ LEVEL ADJ DEBUG\$4)) AND (VHDL OR RTL OR HDL))	USPAT 2000/08/28 09:38
0	rtl same observability	USPAT 2000/08/28 09:38
6	((((SOURCE ADJ LEVEL ADJ DEBUG\$4)) AND (RTL))	USPAT 2000/08/28 09:39
6	rtl and observability	USPAT 2000/08/28 10:43
50	gate adj level adj simulation	USPAT 2000/08/28 10:44
3	(gate adj level adj simulation) same rtl	USPAT 2000/08/28 10:47
0	(gate adj level adj simulation) same breakpoint	USPAT 2000/08/28 10:48
0	(gate adj level adj simulation) same (break adj point\$1)	USPAT 2000/08/28 10:48
2	(gate adj level adj simulation) and (break adj point\$1)	USPAT 2000/08/28 10:48
3	(gate adj level adj simulation) and breakpoint	USPAT 2000/08/28 10:48

NPL Search

IEL – RTL and simulat* and observability
RTL and debug*
source <word> level and debug*
gate <word> level <word> simulation and synthesis

Consultation

Bill Thomson – he examined related case 09/122,493

Search for Application Number

Background Info

Effective Filing Date: 09/127,584

Inventor: Raynaud et al.

Assignee: Mentor Graphics

Title: Method for Gate Level Simulation of Synthesized RTL Designs with Source Level Debugging

Search

Search: First

Date: 1/24/00

Patent Search

Classes/Subclasses

395/500.35, 500.36, 500.37

714/724, 734

East Search

0	(RTL adj source adj code)	USPAT 2000/01/24 10:31
2	(RTL near3 debug\$4)	USPAT 2000/01/24 10:33
1	((RTL SAME DEBUG\$4) AND BREAKPOINT)	USPAT 2000/01/24 10:35
29	(RTL AND ((SIMULAT\$3 NEAR CIRCUIT)) AND DEBUG\$4)	USPAT 2000/01/24 10:36
0	((RTL AND ((SIMULAT\$3 NEAR CIRCUIT)) AND DEBUG\$4)) and breakpoint	USPAT 2000/01/24 10:36
22	((((RTL AND ((SIMULAT\$3 NEAR CIRCUIT)) AND DEBUG\$4)) AND BREAK)	USPAT 2000/01/24 10:36
40	(SOURCE ADJ LEVEL ADJ DEBUG\$4)	USPAT 2000/01/24 14:07
5	((((SOURCE ADJ LEVEL ADJ DEBUG\$4)) AND (VHDL OR RTL OR HDL))	USPAT 2000/01/24 14:14
3	((((SOURCE ADJ LEVEL ADJ DEBUG\$4)) AND (circuit adj simulat\$3))	USPAT 2000/01/24 14:15

NPL Search

IEL – source and level and debug*, RTL and debug*

ACM – RTL and debug

Our Reference: 02282.P055

Patent

METHOD AND APPARATUS FOR GATE-LEVEL SIMULATION OF SYNTHESIZED REGISTER TRANSFER LEVEL DESIGNS WITH SOURCE-LEVEL DEBUGGING

Inventors: Alain Raynaud and Luc M. Burgun

Respectfully submitted,

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1551 U.S. PTO
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Michelle J. Turner

(Typed or printed name of person mailing paper or fee)

(Signature of person mailing paper or fee)

(Date signed)

Serial/Patent No.: <u>****</u>	Filing/Issue Date: <u>July 31, 1998</u>
Client: <u>Mentor Graphics (Raynaud, et al.)</u>	
Title: <u>Method and Apparatus for Gate-Level Simulation of Synthesized Register Transfer Level Designs with Source-Level Debugging</u>	
BSTZ File No.: <u>02282.P055</u>	Atty/Secty Initials: <u>WDD/mjt</u>
Date Mailed: <u>July 31, 1998</u>	Docket Due Date: <u>*****</u>
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<input type="checkbox"/> Amendment/Response (____ pgs.)	<input checked="" type="checkbox"/> Express Mail No.: <u>EM542801726US</u> <input checked="" type="checkbox"/> Check No. <u>5412</u>
<input checked="" type="checkbox"/> Appeal Brief (____ pgs.) (in triplicate)	<input type="checkbox"/> _____ Month(s) Extension of Time Amt: <u>\$1568.00</u>
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<input type="checkbox"/> Application - Rule 1.62 Transmittal (____ pgs.)	<input checked="" type="checkbox"/> Petition for _____
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<input type="checkbox"/> Disclosure Docs & Orig & Copy of Inventor's Signed Letter (____ pgs.)	<input type="checkbox"/> Small Entity Declaration for Indep. Inventor/Small Business
<input checked="" type="checkbox"/> Drawings: <u>20</u> # of sheets includes <u>22</u> figures	<input checked="" type="checkbox"/> Transmittal Letter (original & copy) x 1 page each
<input checked="" type="checkbox"/> Other: Fee transmittal (original & copy) x 1 page each	